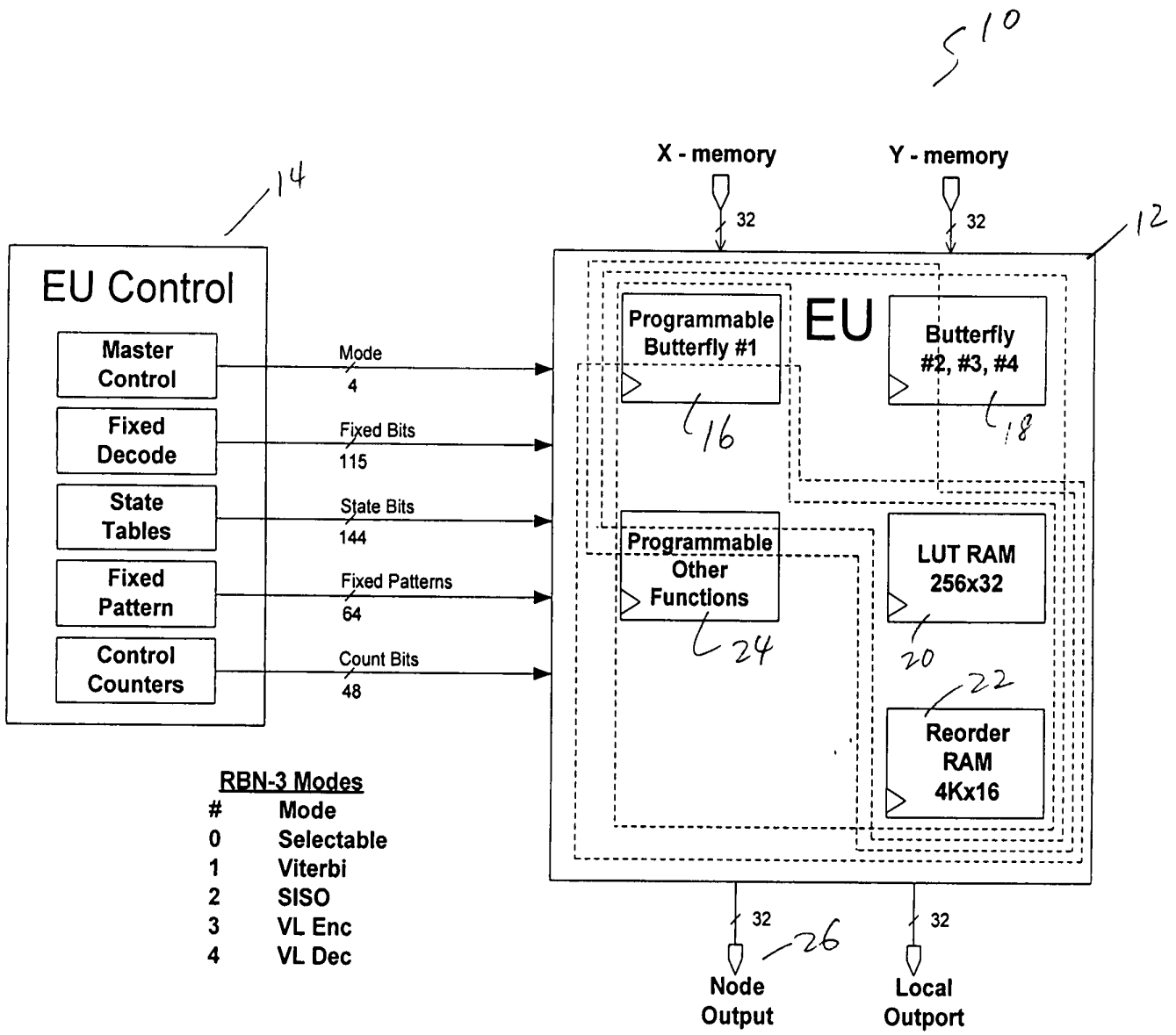

10
14
EU Control
Master Control
Fixed Decode
State Tables
Fixed Pattern
Control Counters
Mode
4
Fixed Bits
115
State Bits
144
Fixed Patterns
64
Count Bits
48
X - memory
Y - memory
32
32
12
EU
Programmable Butterfly #1
16
Butterfly #2, #3, #4
18
Programmable Other Functions
24
LUT RAM 256x32
20
22
Reorder RAM 4Kx16
32
32
26
Node Output
Local Outport
RBN-3 Modes
Mode
0 Selectable
1 Viterbi
2 SISO
3 VL Enc
4 VL Dec

Fig. 1A

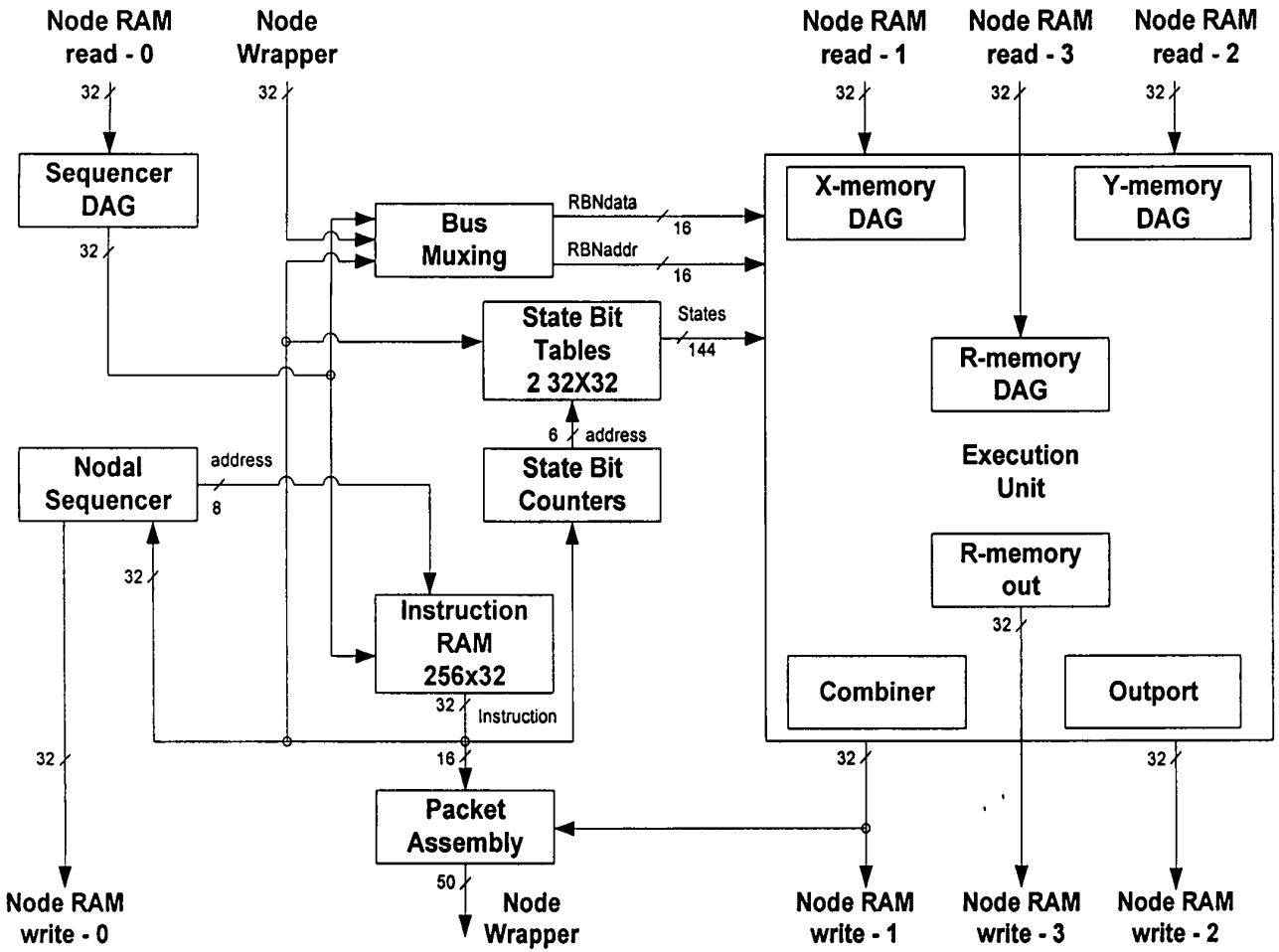

Node RAM read - 0
Node Wrapper
Node RAM read - 1
Node RAM read - 3
Node RAM read - 2
32
Sequencer DAG
Bus Muxing
RBNdata
RBNaddr
16
X-memory DAG
Y-memory DAG
State Bit Tables 2 32X32
States
144
R-memory DAG
6
address
Nodal Sequencer
address
8
State Bit Counters
Execution Unit
R-memory out
Instruction RAM 256x32
Instruction
Combiner
Outport
Packet Assembly
50
Node RAM write - 0
Node Wrapper
Node RAM write - 1
Node RAM write - 3
Node RAM write - 2

Fig. 1B

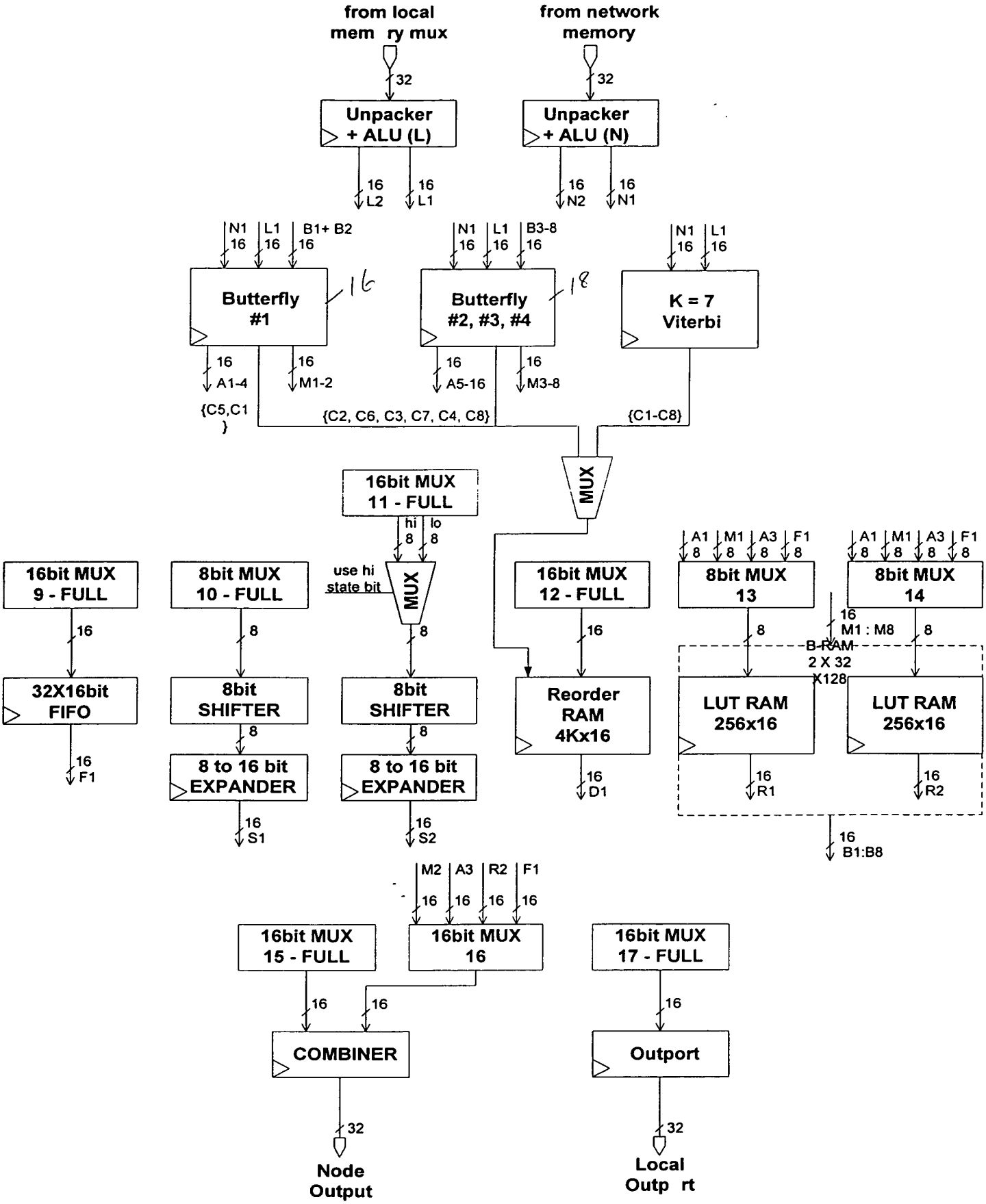
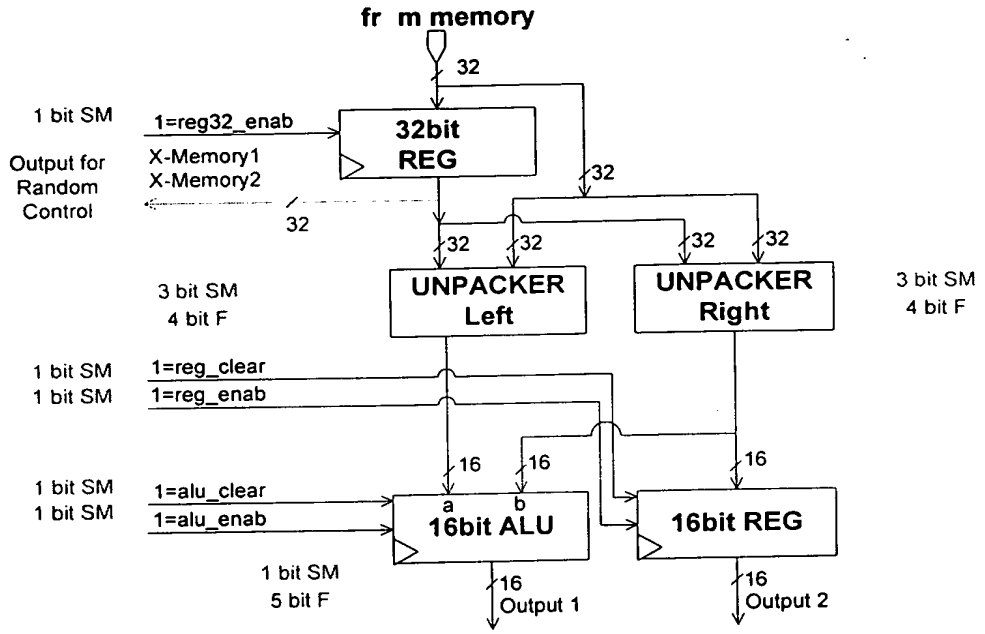

from local mem ry mux
from network memory
32
32
Unpacker + ALU (L)
Unpacker + ALU (N)
16 L2
16 L1
16 N2
16 N1
N1 16
L1 16
B1+ B2 16
N1 16
L1 16
B3-8 16
N1 16
L1 16
Butterfly #1
16
Butterfly #2, #3, #4
18
K = 7 Viterbi
16 A1-4
16 M1-2
16 A5-16
16 M3-8
{C5,C1}
{C2, C6, C3, C7, C4, C8}
{C1-C8}
MUX
16bit MUX 11 - FULL
hi 8
lo 8
use hi state bit
MUX
16bit MUX 9 - FULL
8bit MUX 10 - FULL
16bit MUX 12 - FULL
A1 8
M1 8
A3 8
F1 8
8bit MUX 13
A1 8
M1 8
A3 8
F1 8
8bit MUX 14
16 M1 : M8
B-RAM 2 X 32 X128
32X16bit FIFO
8bit SHIFTER
8bit SHIFTER
Reorder RAM 4Kx16
LUT RAM 256x16
LUT RAM 256x16
16 F1
8 to 16 bit EXPANDER
8 to 16 bit EXPANDER
16 S1
16 S2
16 D1
16 R1
16 R2
16 B1:B8
M2 16
A3 16
R2 16
F1 16
16bit MUX 15 - FULL
16bit MUX 16
16bit MUX 17 - FULL
COMBINER
Outport
32
32
Node Output
Local Outp rt

Fig. 2

Unpacker + ALU

Total: 13 bit F

Total: 12 bit SM



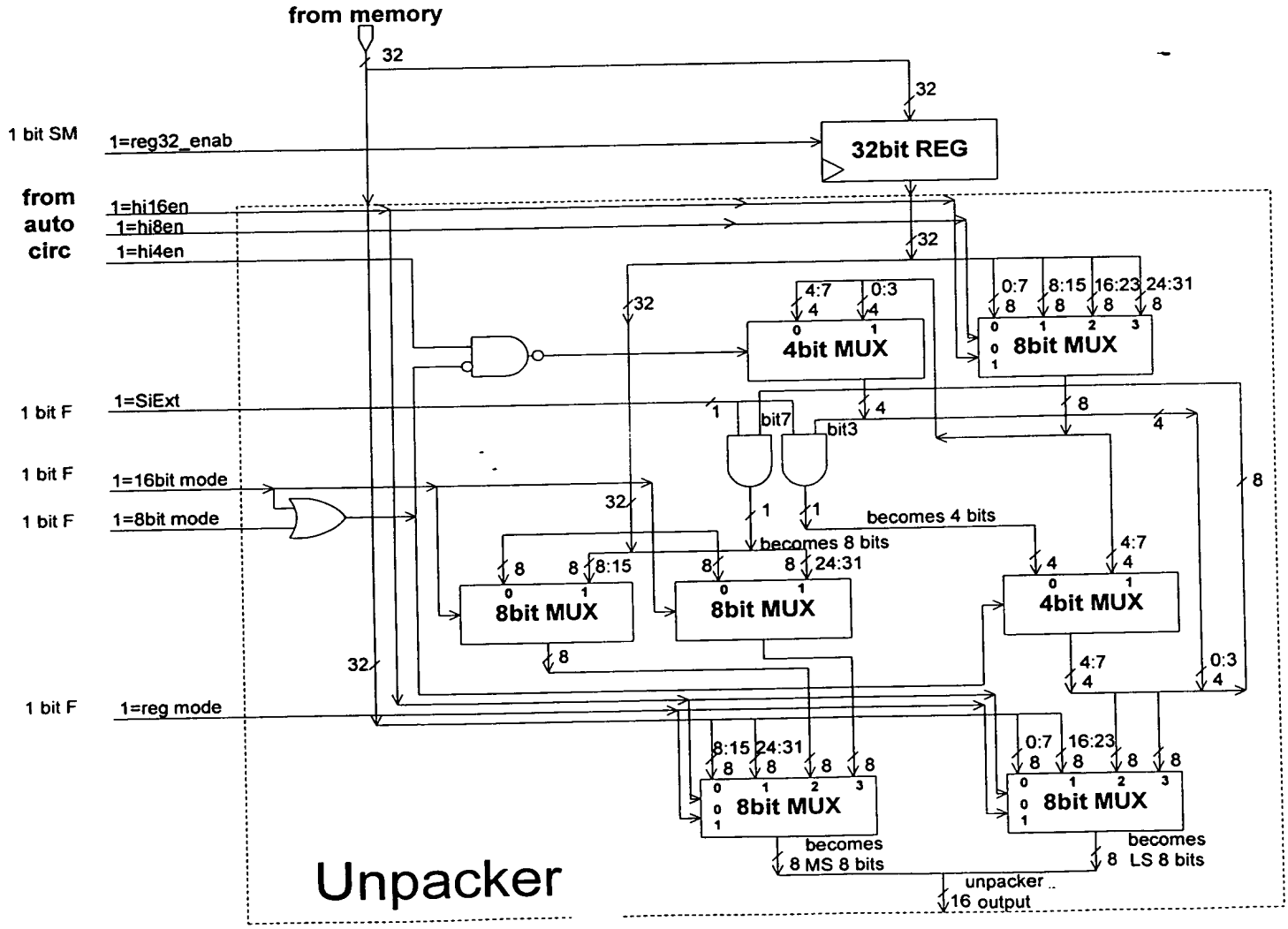


Fig- 3

32 X 16 bit
Register File

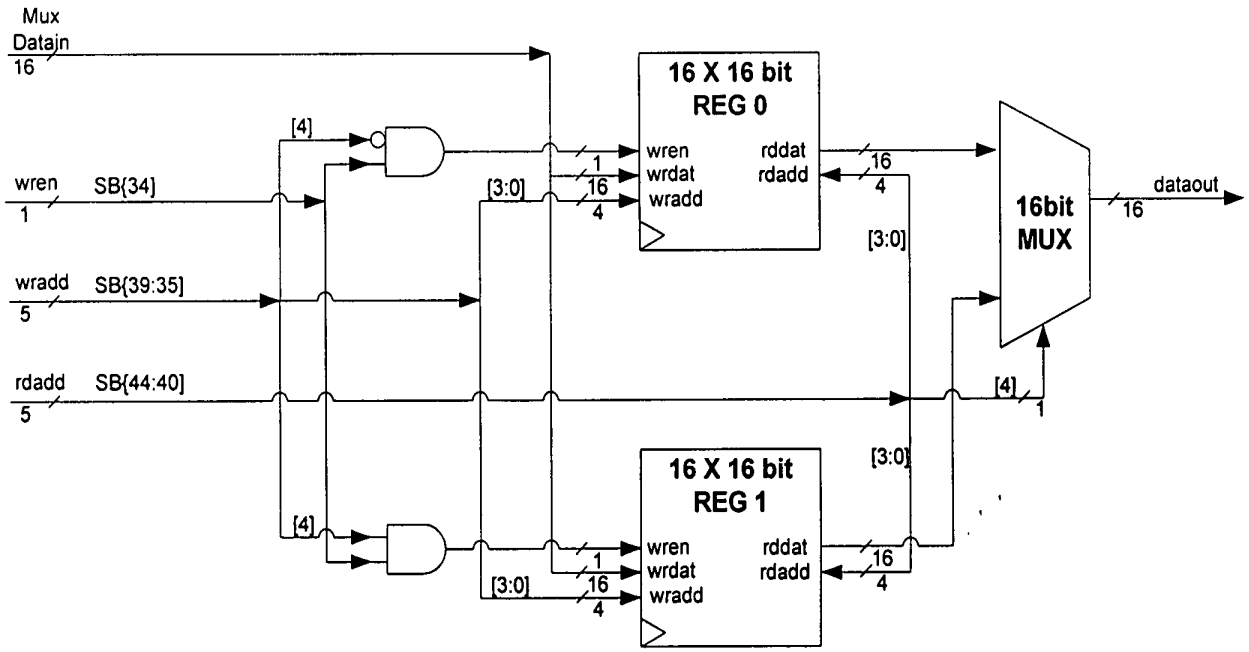
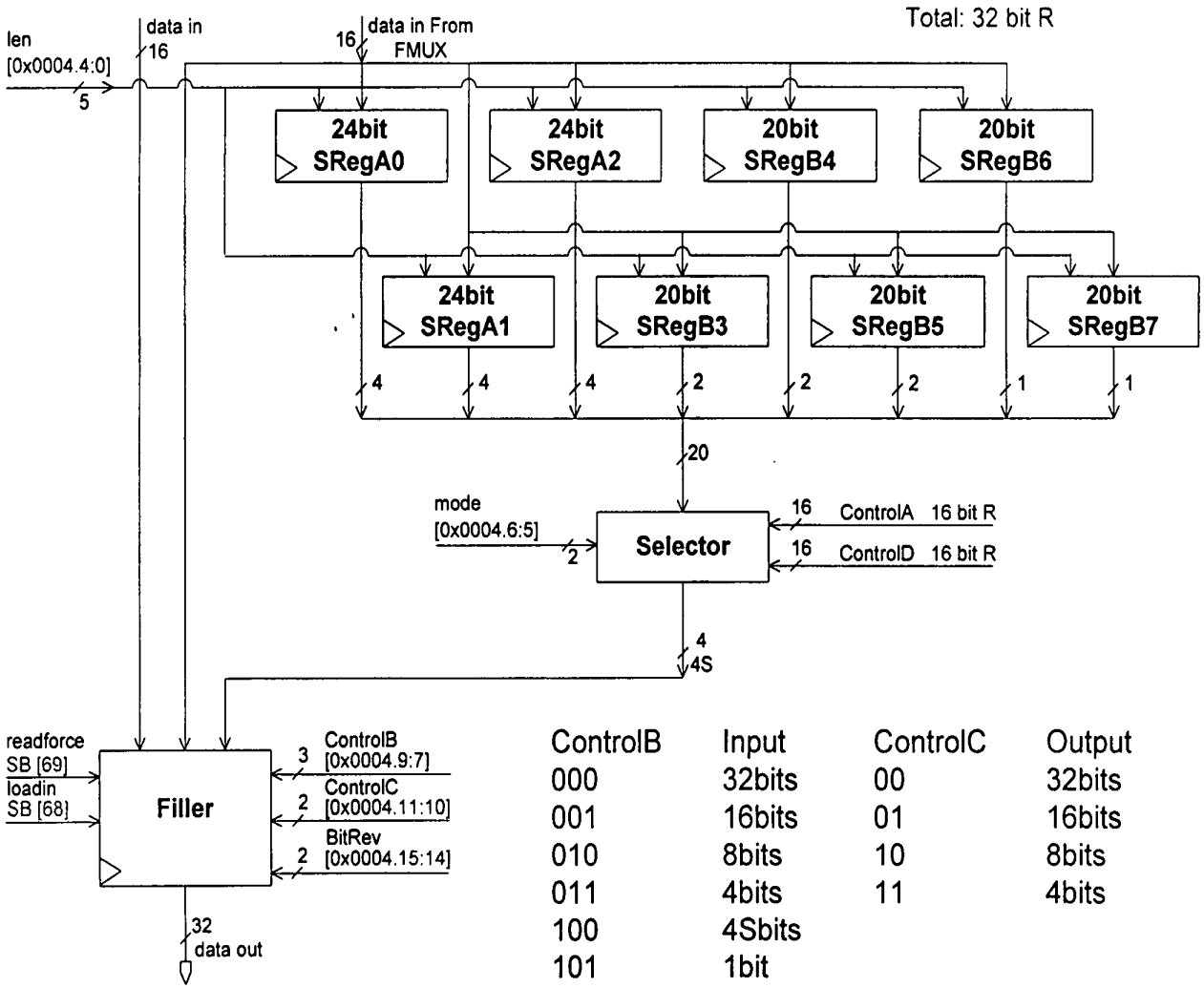


Fig. 4

32 bit Combiner



ControlB	Input	ControlC	Output
000	32bits	00	32bits
001	16bits	01	16bits
010	8bits	10	8bits
011	4bits	11	4bits
100	4Sbits		
101	1bit		
110	unused		
111	unused		

Fig. 5

Butterfly #1

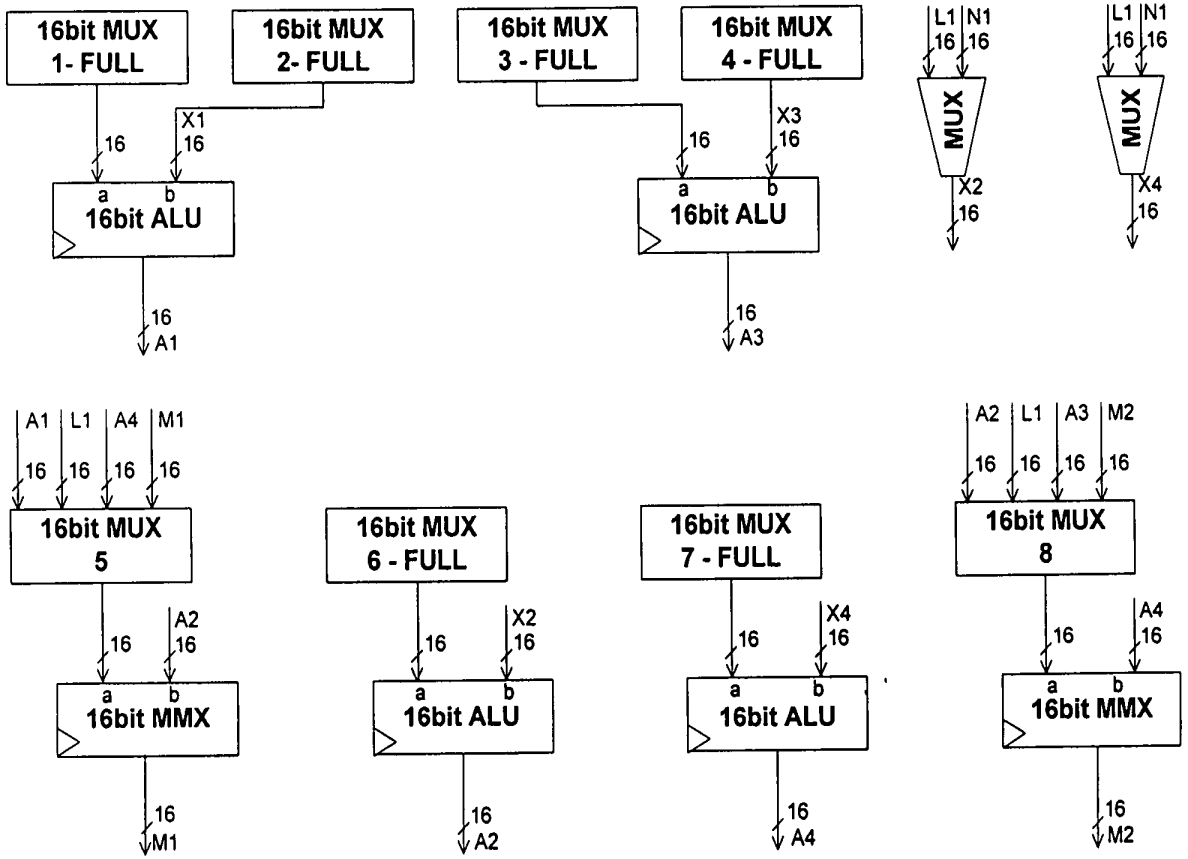


Fig. 6A

Dual ACS Unit (Butterfly)

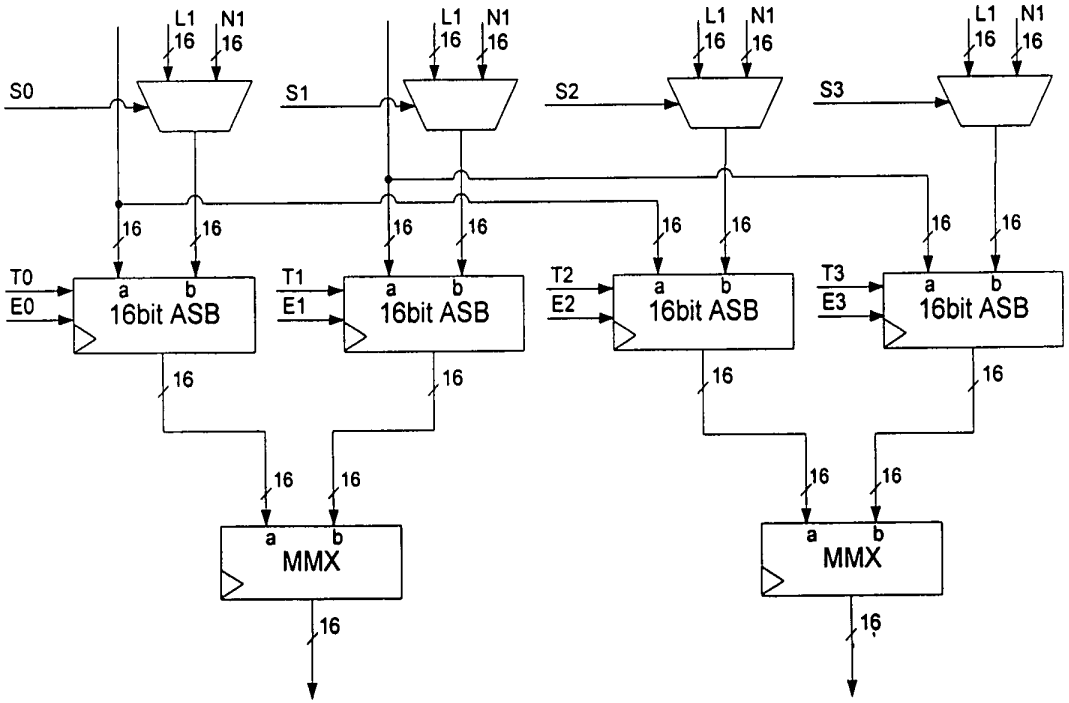


Fig. 6B

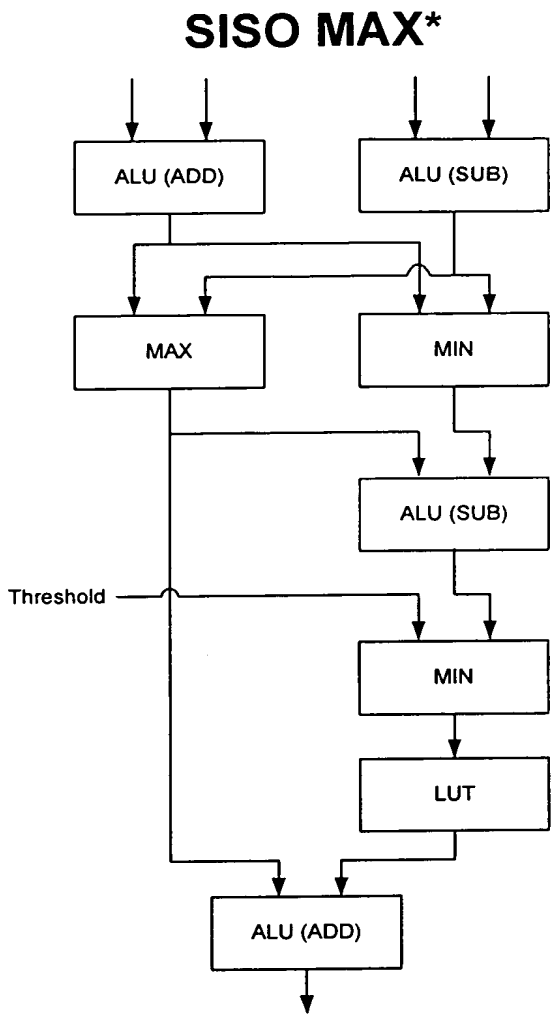

SISO MAX*
ALU (ADD)
ALU (SUB)
MAX
MIN
ALU (SUB)
Threshold
MIN
LUT
ALU (ADD)

Fig. 7A

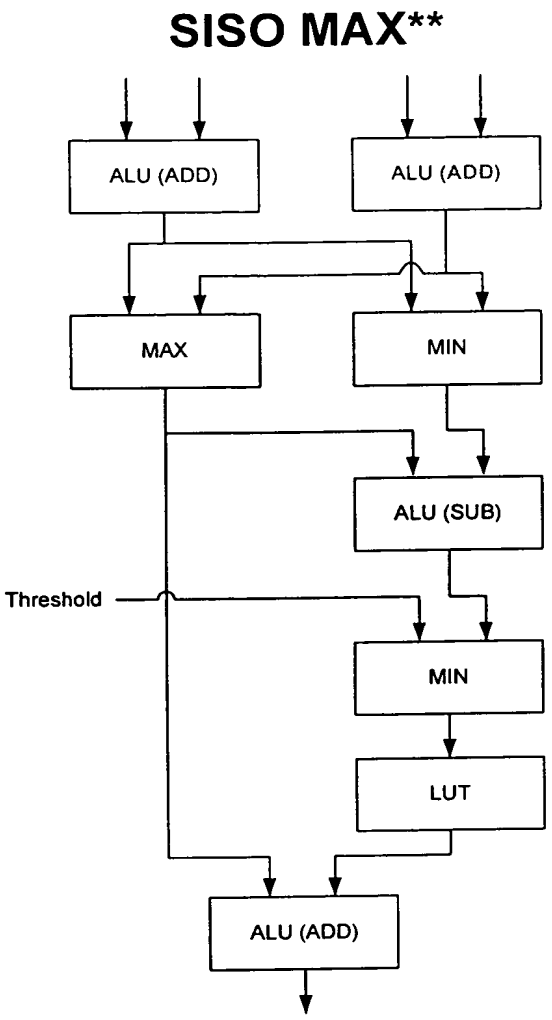
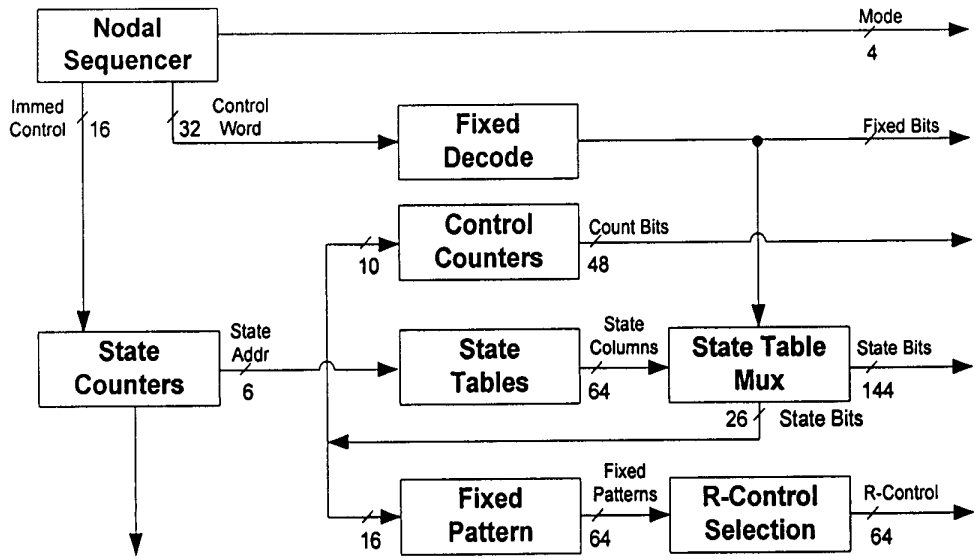

SISO MAX**
ALU (ADD)
ALU (ADD)
MAX
MIN
ALU (SUB)
Threshold
MIN
LUT
ALU (ADD)

Fig. 7B

Simplified RBN -3 Control



RBN-3 Control Types

#	Type
0	Fixed
1	State Machine
2	R-Control

RBN-3 Control Modes

#	Mode	Fixed	State	R-Control
0	Selectable	X	X	X
1	Viterbi	X	X	X
2	SISO	X	X	X
3	VL Enc	X	X	
4	VL Dec	X	X	

Fig. 8A

RBN-3 Control

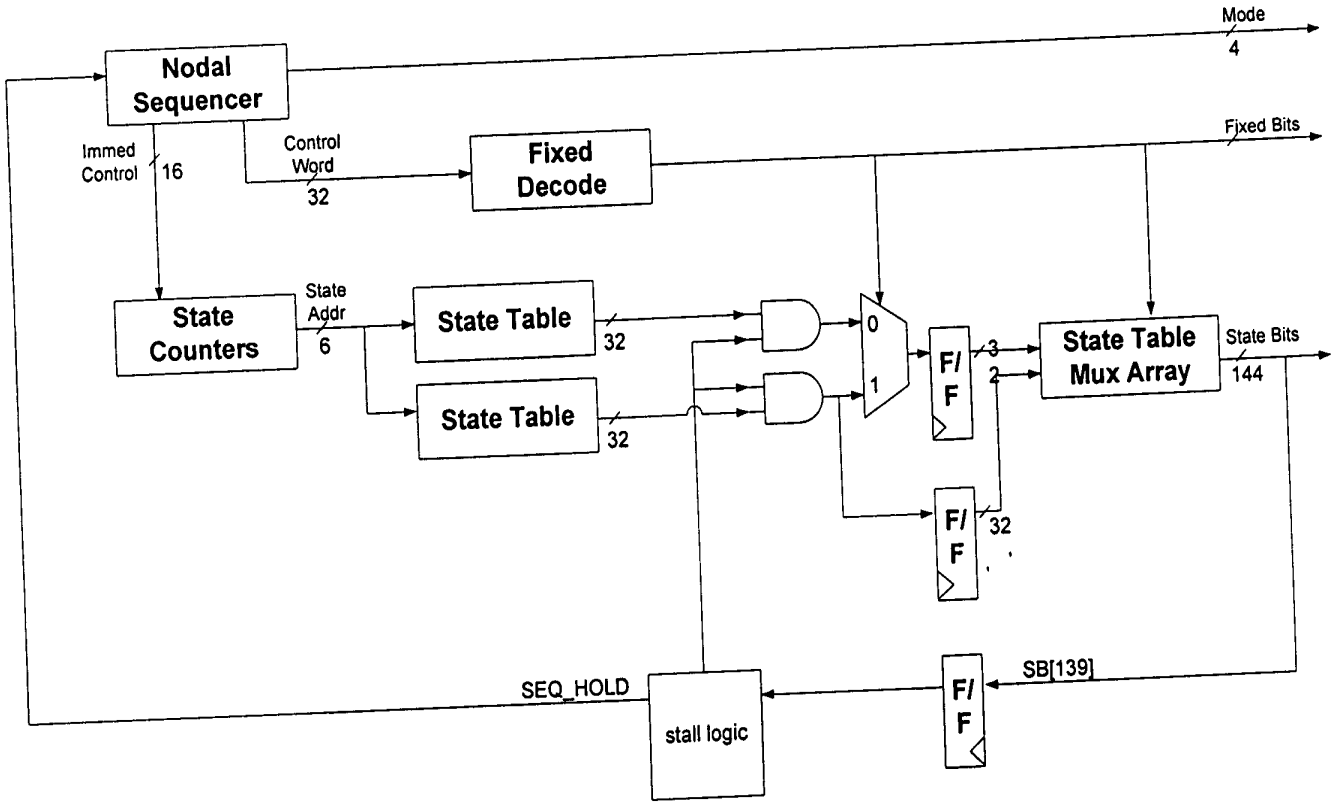


Fig. 8B

Programmable Pattern Generator

Possible Outputs

Sel Code							
00	1/5	2/5	3/5	4/5			
01	1/6	1/3	1/2	2/3	5/6		
10	1/7	2/7	3/7	4/7	5/7	6/7	
11	1/8	1/4	3/8	1/2	5/8	3/4	7/8

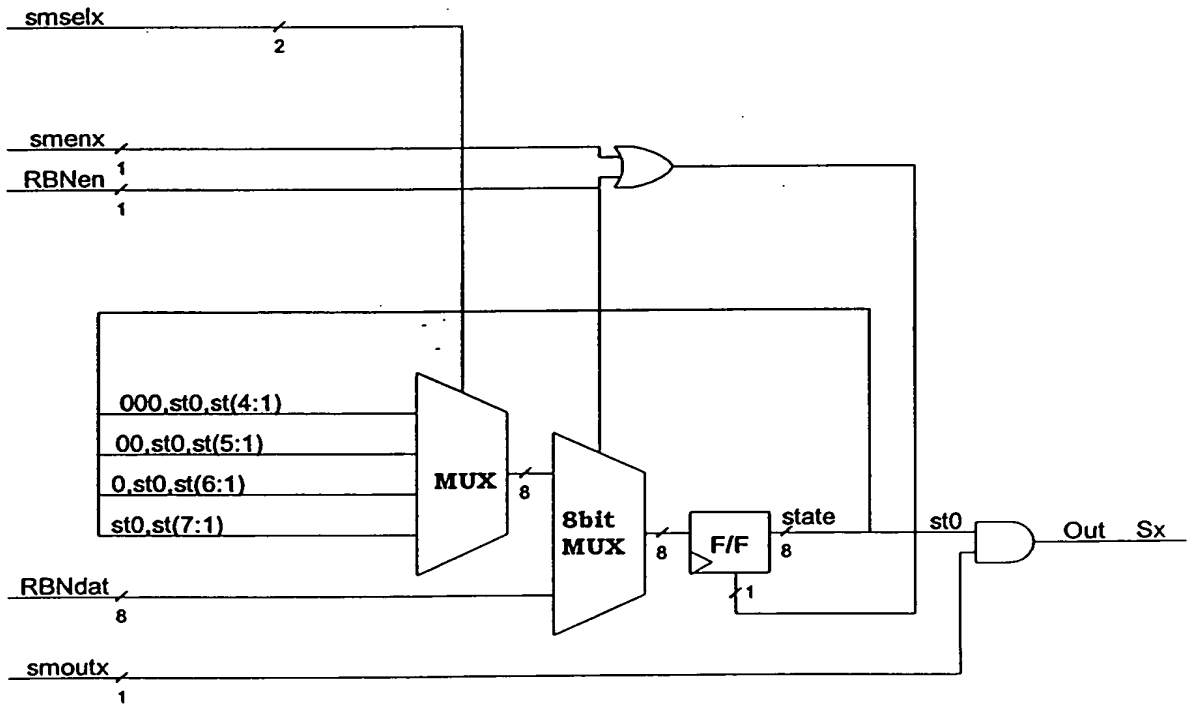


Fig. 9

State Bit Table

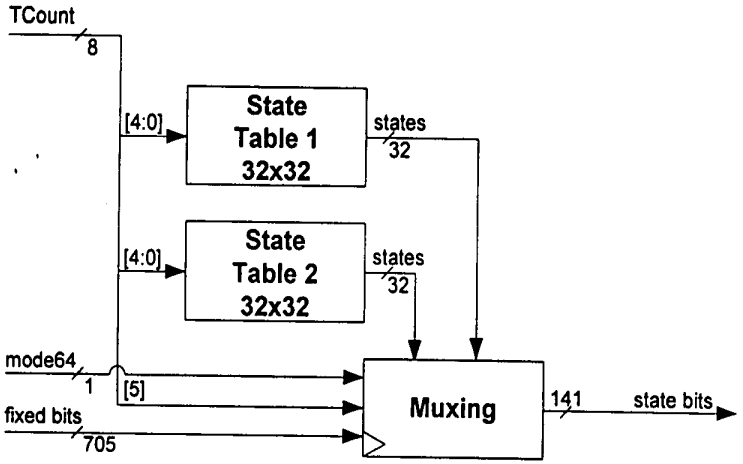


Fig. 10A

State Bit Table Counters

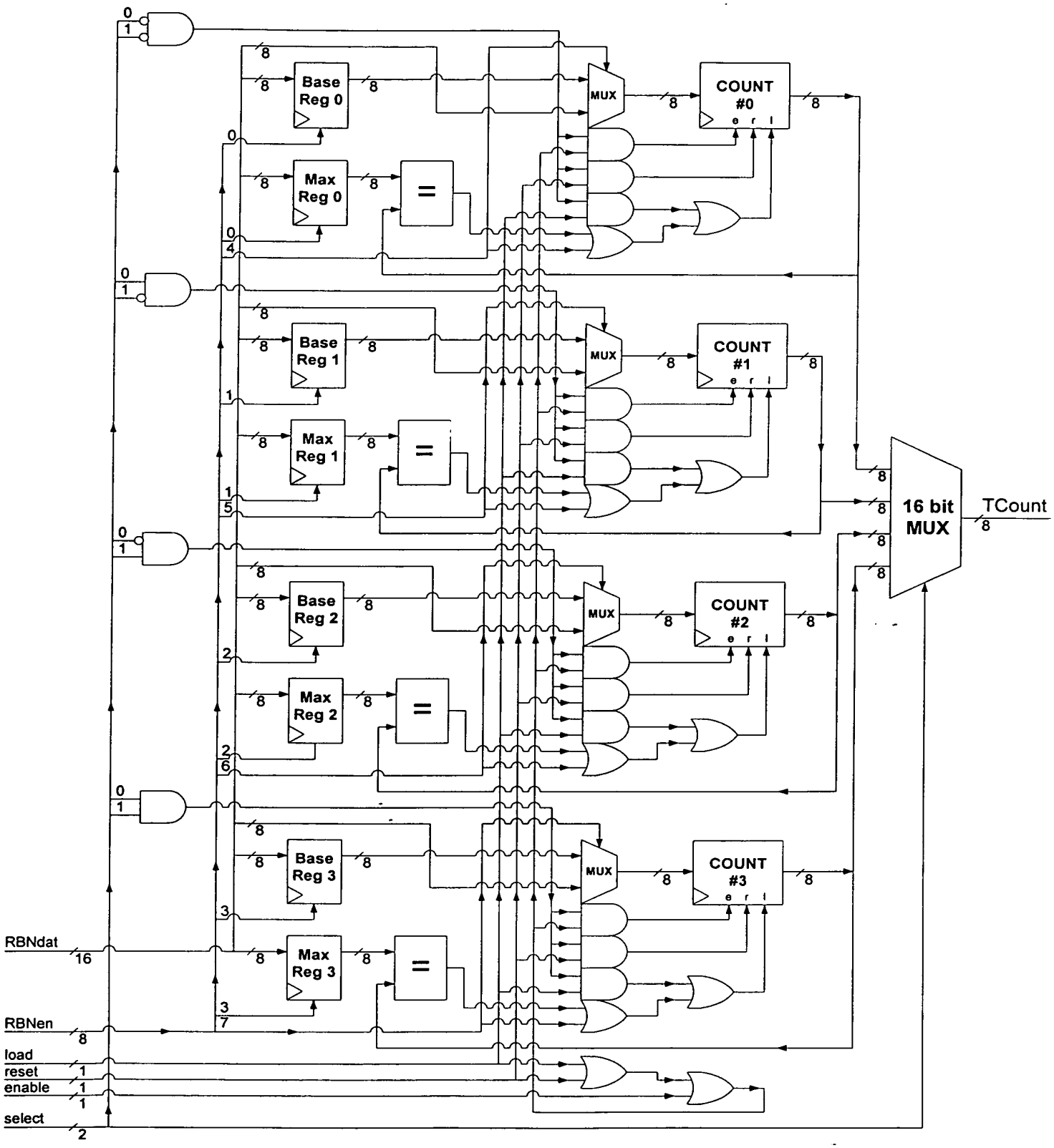
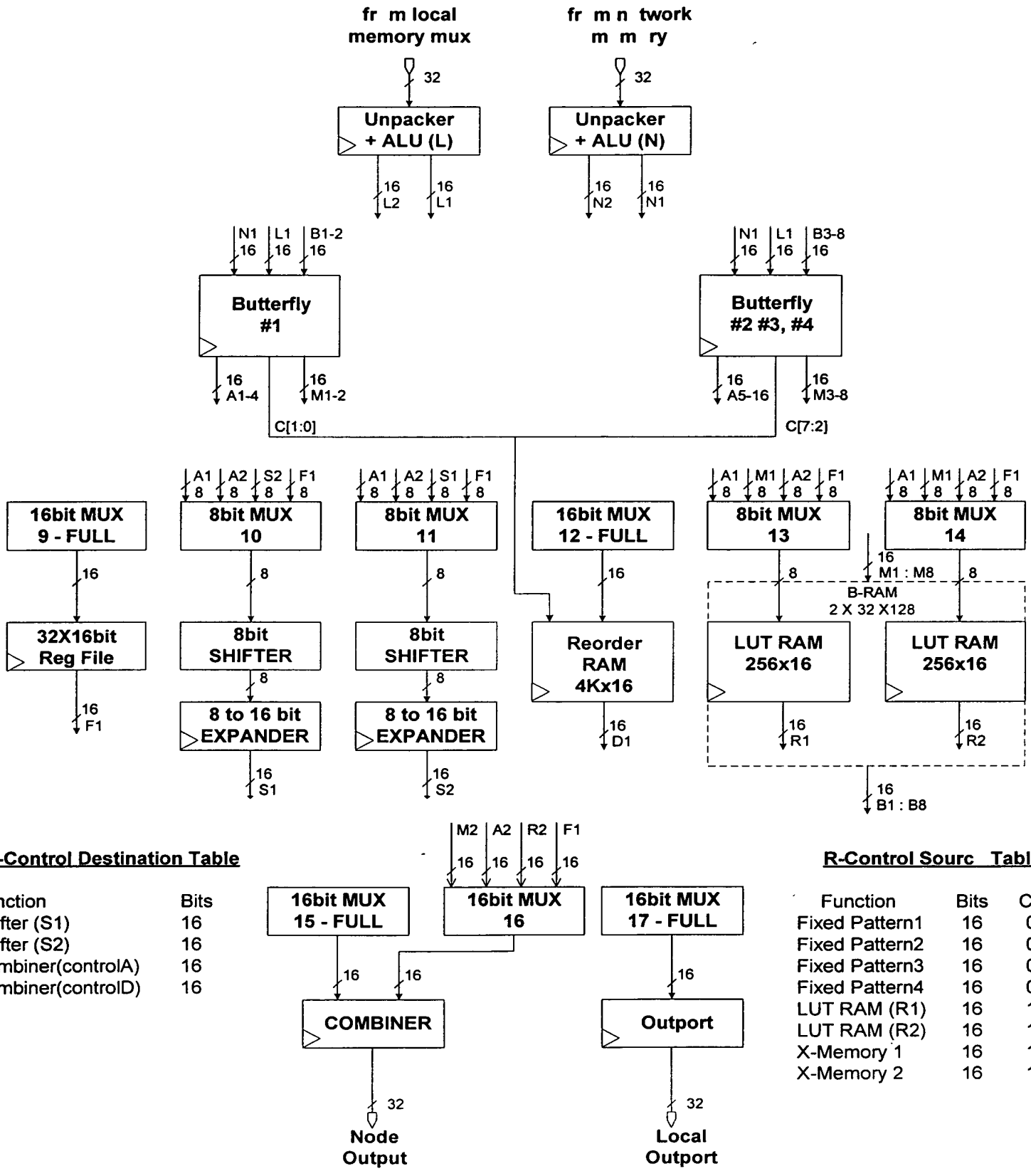


Fig. 10B

RBN-3 R -Control



R-Control Destination Table

Function	Bits
Shifter (S1)	16
Shifter (S2)	16
Combiner(controlA)	16
Combiner(controlD)	16

R-Control Sourc Table

Function	Bits	Code
Fixed Pattern1	16	000
Fixed Pattern2	16	001
Fixed Pattern3	16	010
Fixed Pattern4	16	011
LUT RAM (R1)	16	100
LUT RAM (R2)	16	101
X-Memory 1	16	110
X-Memory 2	16	111

Fig-11

Fixed Pattern Control

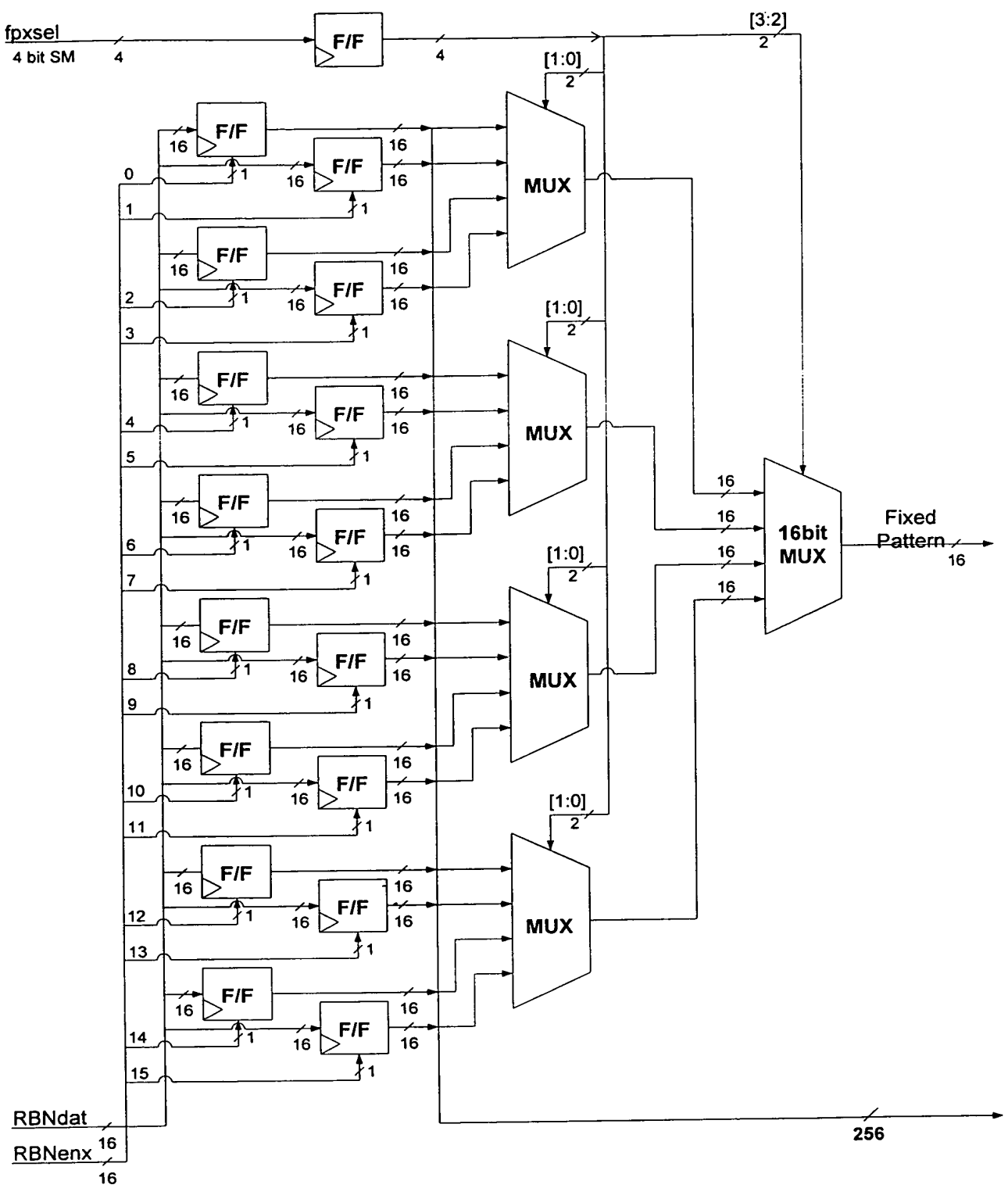


Fig. 12

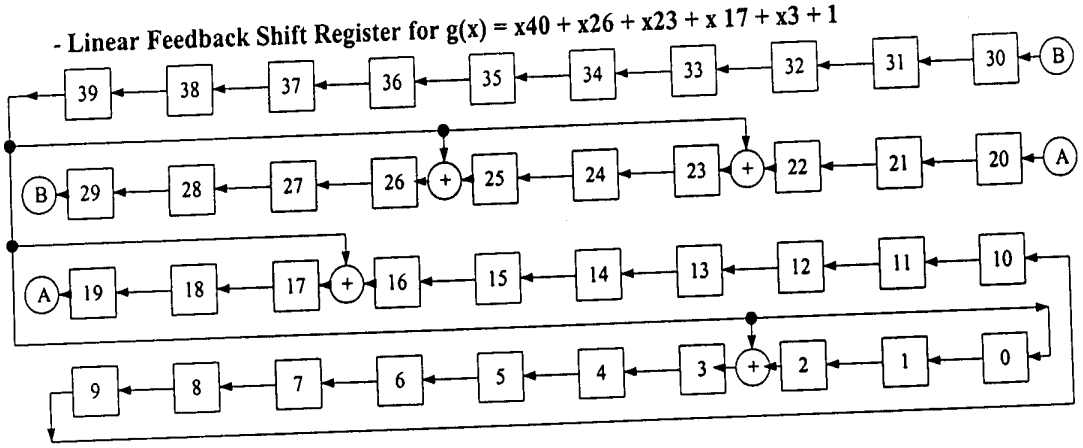

- Linear Feedback Shift Register for g(x) = x40 + x26 + x23 + x 17 + x3 + 1
39
38
37
36
35
34
33
32
31
30
B
29
28
27
26
25
24
23
22
21
20
A
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0

Fig. 13

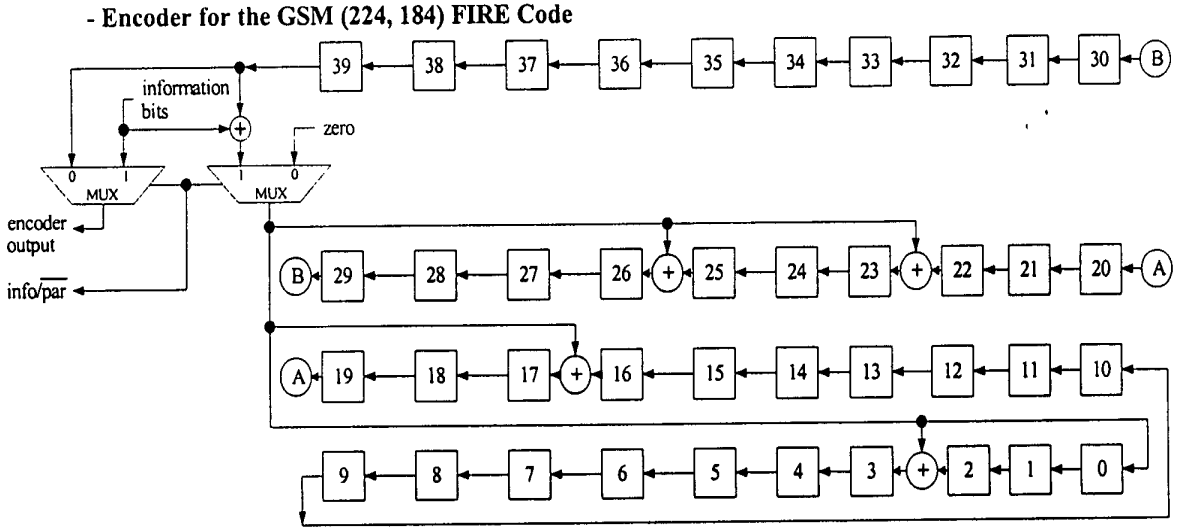

- Encoder for the GSM (224, 184) FIRE Code
information bits
zero
MUX
MUX
encoder output
info/par
39
38
37
36
35
34
33
32
31
30
B
29
28
27
26
25
24
23
22
21
20
A
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0

Fig. 14

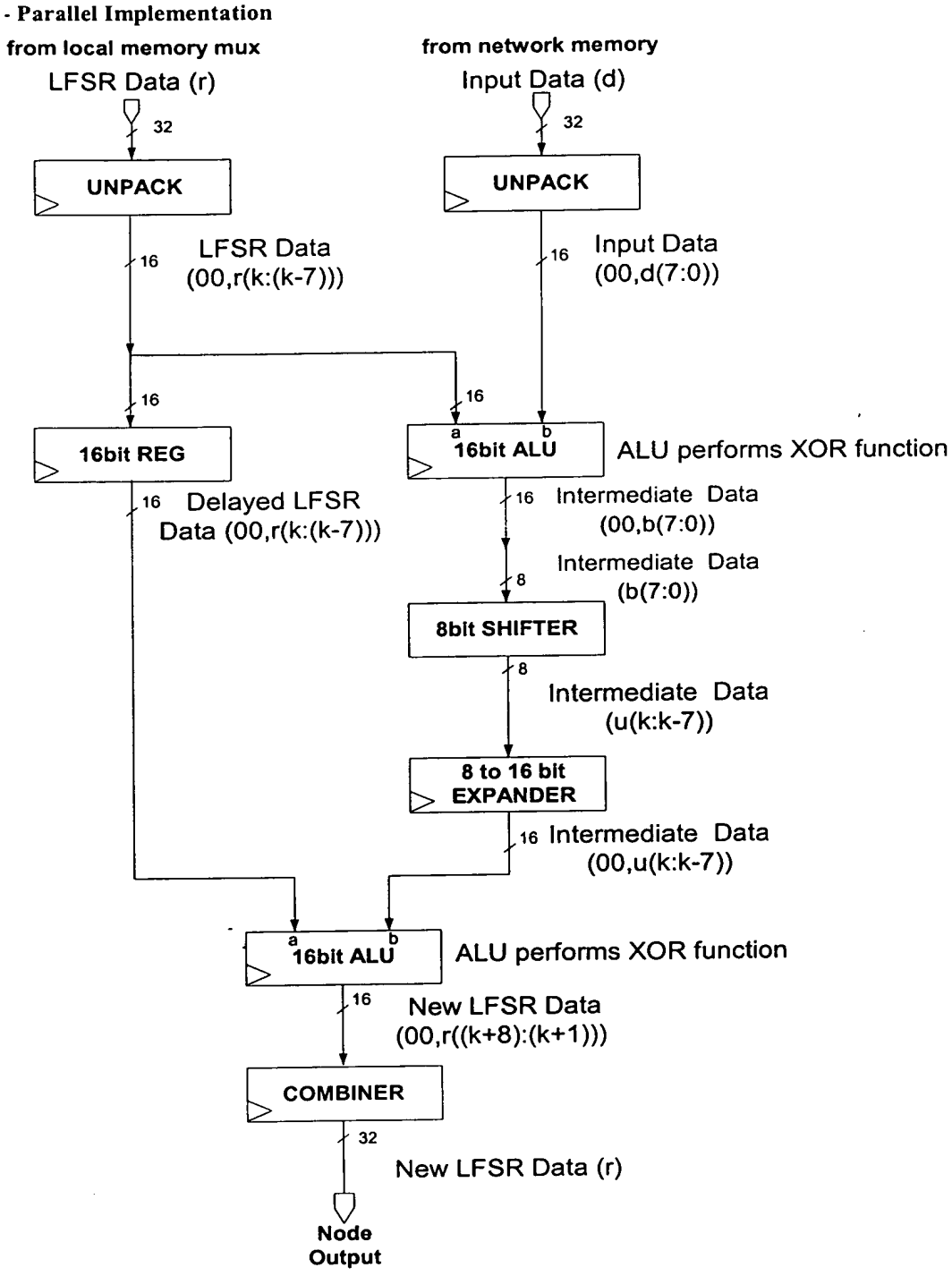
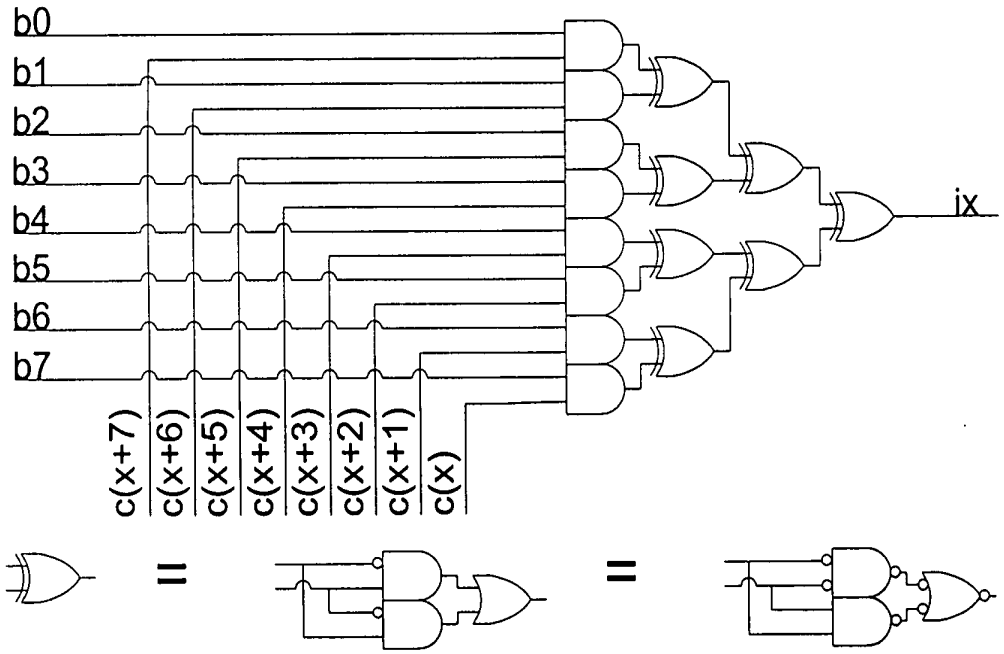

- Parallel Implementation
from local memory mux
LFSR Data (r)
32
UNPACK
16
LFSR Data
(00,r(k:(k-7)))
from network memory
Input Data (d)
32
UNPACK
16
Input Data
(00,d(7:0))
16
16
16bit REG
a
b
16bit ALU
ALU performs XOR function
16
Delayed LFSR
Data (00,r(k:(k-7)))
16
Intermediate Data
(00,b(7:0))
8
Intermediate Data
(b(7:0))
8bit SHIFTER
8
Intermediate Data
(u(k:k-7))
8 to 16 bit
EXPANDER
16
Intermediate Data
(00,u(k:k-7))
a
b
16bit ALU
ALU performs XOR function
16
New LFSR Data
(00,r((k+8):(k+1)))
COMBINER
32
New LFSR Data (r)
Node
Output

Fig. 15

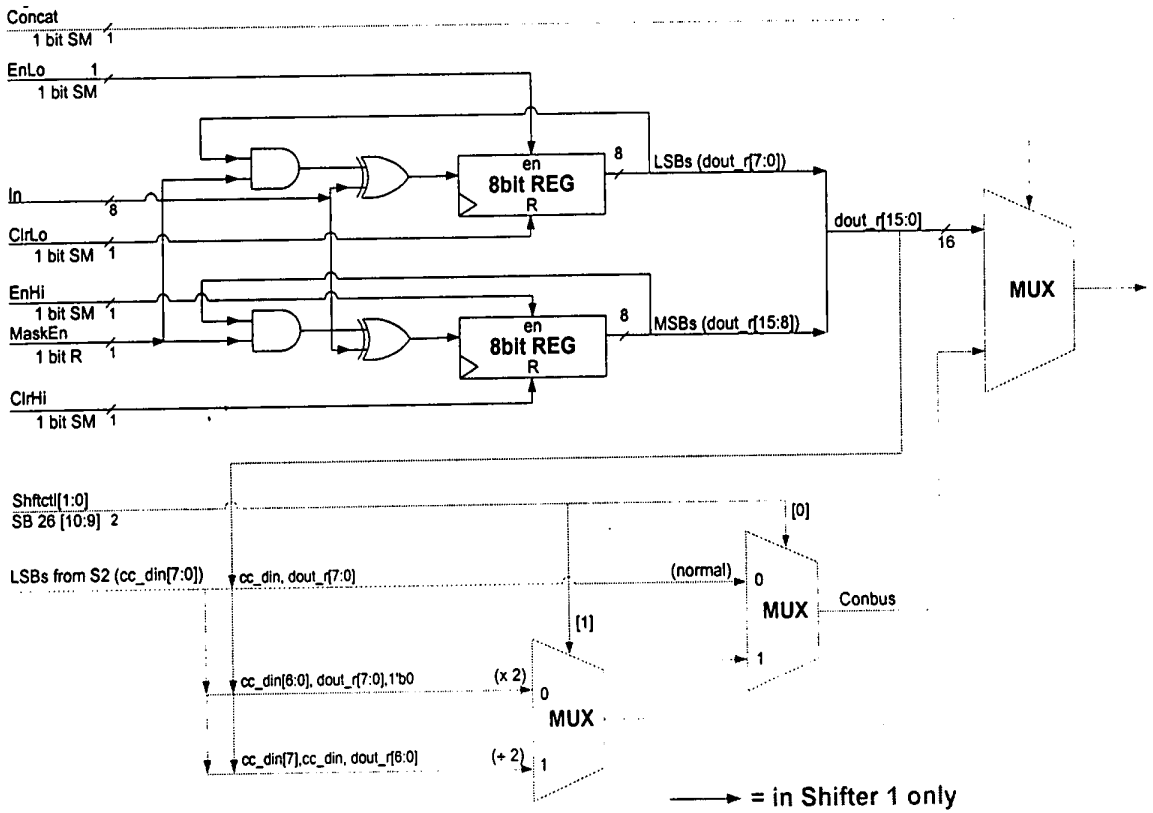
- Bit Shifter



Out	In	Control
i0	b(7:0)	c(7:0)
i1	b(7:0)	c(8:1)
i2	b(7:0)	c(9:2)
i3	b(7:0)	c(10:3)
i4	b(7:0)	c(11:4)
i5	b(7:0)	c(12:5)
i6	b(7:0)	c(13:6)
i7	b(7:0)	c(14:7)

Fig. 16

- 8 to 16 bit Expander



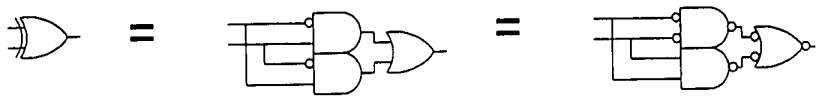


Fig. 17

- Linear Feedback Shift Register for g(x) = x18 + x10 + x5 + 1

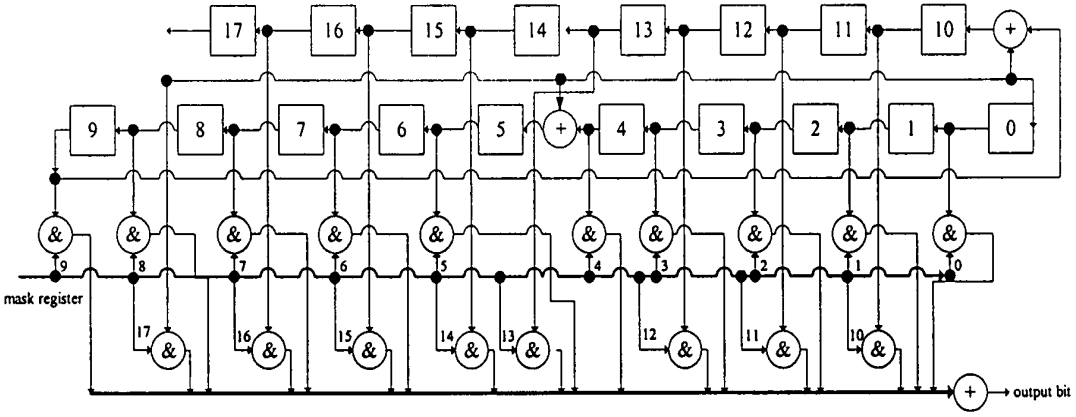


Fig. 18